

AMENDMENTS TO THE CLAIMS

Please amend claims 1-20 as follows:

Listing of the Claims:

1. (Currently Amended) A semiconductor component comprising a stress-absorbing semiconductor layer, having:

a carrier material (1);

a crystalline stress generator layer (SG) which is formed on the carrier material (1) and substantially has a first lattice constant, for generating a mechanical stress;

an insulating stress transmission layer (2) which is formed on the stress generator layer (SG) and is used to transmit the mechanical stress which is generated;

a crystalline, stress-absorbing semiconductor layer (SA) which is formed on the stress transmission layer (2) and has a second lattice constant, which is different than the first lattice constant, for absorbing the mechanical stress which has been generated and transmitted and for realizing source/drain regions (S, D) and a channel region (K);

a gate dielectric (3) which is formed at least at the surface of the channel region (K); and

a control layer (4) for driving the channel region (K), which is formed on the gate dielectric (3).

2. (Currently Amended) The semiconductor component as ~~elaimed in patent~~ recited in claim 1, wherein the stress-absorbing semiconductor layer (SA) has a thickness (d) less than 1/3 of a length (L) of the channel region (K).

3. (Currently Amended) The semiconductor component as ~~elaimed in patent claim 1 or 2~~ recited in claim 1, wherein the stress transmission layer (2) forms a crystalline insulator layer.

4. (Currently Amended) The semiconductor component as ~~elaimed in patent~~ recited in claim 3, wherein the stress transmission layer (2) has a lattice constant which is matched to the second lattice constant of the stress-absorbing semiconductor layer (SA).

5. (Currently Amended) The semiconductor component as ~~claimed in one of patent claims 1 to 4~~ recited in claim 1, wherein the stress generator layer (SG) is an approx. 10 to 300 nm thick SiGe layer, the stress transmission layer (2) is an approx. 1 to 2 nm thick CaF₂ layer, and the stress-absorbing semiconductor layer (SA) is an approx. 5 nm thick Si layer.

6. (Currently Amended) The semiconductor component as ~~claimed in one of patent claims 1 to 5~~ recited in claim 1, wherein the gate dielectric (3) ~~has~~ is formed from a material having a high dielectric constant.

7. (Currently Amended) The semiconductor component as ~~claimed in one of patent claims 1 to 6~~ recited in claim 1, wherein the control layer (4) includes a metal.

8. (Currently Amended) The semiconductor component as ~~claimed in one of patent claims 1 to 7~~ recited in claim 1, wherein the carrier material (1) ~~includes further~~ comprises:

[an] a Si substrate (1A) with a (100) surface orientation, and

[an] a Si buffer layer (1B) for generating a flat starting surface for the stress generator layer (SG).

9. (Currently Amended) A method for fabricating a semiconductor component ~~with~~ having a stress-absorbing semiconductor layer, comprising the steps of:

- a) forming a carrier material (1);
- b) forming a crystalline stress generator layer (SG) having substantially a first lattice constant on the carrier material (1) in order to generate a mechanical stress;
- c) forming an insulating stress transmission layer (2) on the stress generator layer (SG) for transmitting the mechanical stress ~~which~~ that has been generated;
- d) forming a crystalline, stress-absorbing semiconductor layer (SA) having a second lattice constant, which is different than the first lattice constant, on the stress transmission layer (2) for the purpose of absorbing the mechanical stress;
- e) forming a gate dielectric (3) on the stress-absorbing semiconductor layer (SA);
- f) forming a control layer (4) on the gate dielectric (3);

- g) patterning the gate dielectric (3) and the control layer (4); and
 - h) forming source/drain regions (S, D) in the stress-absorbing semiconductor layer (SA).
10. (Currently Amended) The method as ~~claimed in patent~~ recited in claim 9, wherein in step a) [a] the semiconductor substrate (~~1A~~) having a (100) surface orientation is provided, and a semiconductor buffer layer (~~1B~~) is epitaxially deposited thereon in order to produce a smooth surface.
11. (Currently Amended) The method as ~~claimed in patent~~ recited in claim 9 ~~or 10~~, wherein in step b) a IV-IV or III-V semiconductor is used.
12. (Currently Amended) The method as ~~claimed in patent~~ recited in claim 11, wherein in step b) a multiple layer sequence is formed as the stress generator layer (SG).
13. (Currently Amended) The method as ~~claimed in one of patent claims 9 to 12~~ recited in claim 9, wherein in step b) the stress generator layer (~~SG~~) is smoothed by ~~means of~~ a molecular beam epitaxy process.
14. (Currently Amended) The method as ~~claimed in one of patent claims 9 to 13~~ recited in claim 9, wherein in step c) a crystalline insulator layer is formed as the stress transmission layer (~~2~~).
15. (Currently Amended) The method as ~~claimed in patent~~ recited in claim 14, wherein in step c) [a] the stress transmission layer (~~2~~) with a lattice constant which is matched to the second lattice constant of the stress-absorbing semiconductor layer (~~SA~~) is formed.
16. (Currently Amended) The method as ~~claimed in patent~~ recited in claim 15, wherein in step c) only a few atom layers of the stress transmission layer are deposited epitaxially on the stress generator layer (~~SG~~).

17. (Currently Amended) The method as ~~claimed in one of patent claims 9 to 16~~
recited in claim 9, wherein in step d) a fully depleted semiconductor material is used.

18. (Currently Amended) The method as ~~claimed in one of patent claims 9 to 17~~
recited in claim 9, wherein in step e) a material with a high dielectric constant is used as
the gate dielectric (3).

19. (Currently Amended) The method as ~~claimed in one of patent claims 9 to 18~~
recited in claim 9, wherein in step f) a metal is used as the control layer (4).

20. (Currently Amended) The method as ~~claimed in one of patent claims 9 to 19~~
recited in claim 9, wherein

in step a) Si is used as the carrier material (1);

in step b) SiGe is used as the stress generator layer (SG);

in step c) CaF₂ is used as the stress transmission layer (2);

in step d) Si is used as the stress-absorbing semiconductor layer (SA);

in step e) HfO₂ is used as the gate dielectric (3); and

in step f) TiN is used as the control layer (4).